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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,928	09/22/2003	Naoki Nakamura	021385A	5138

38834 7590 08/23/2005

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EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,928	NAKAMURA, NAOKI	
	Examiner	Art Unit	
	C. J. Arbes	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) *3 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/274,125.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *hereto*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ehman et al (Pat No. 6,021,050) hereinafter Ehman et al.

Ehmn et al teach *inter alia* a method for making a multi-layered printed circuit board (PcB) having buried a plurality of electronic components or passive elements. A B-stage thermal setting resin can be used to bond adjacent layers of the PcB which layers can comprise an epoxy resin impregnated glass fiber matrix (Cf. Abstract and also Col 2). The term "filler" can be defined as "a substance which adds bulk, strength, weight , viscosity or opacity. Therefore it is submitted that the intermediate layers (18 and 20) which are taught by Ehmn et al to be a B-stage thermal setting resin (Cf Col 2) would respond to applicant's recital of the term "filler" in Claims 1 and 2 of the instant Application. If this definition is accurate and proper within the reasonable scope of the instant specification, the claims are anticipated by Ehman et al. Alternatively as will be shown *infra* it is old and hence obvious to use *inter alia* a non-woven fabric when one wishes to make a multilayer printed circuit board. (Cf e.g. Japan Pat No 07249868 A)

Claims 1 and 2 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Takanaka et al (Japan Pat No. 07249868 A) hereinafter Takanaka et al in view of Ehman et al

Takanaka et al teach a method of making a circuit board which includes providing a prepreg sheet on either side of a circuit board. A metal foil is arranged on either side of the external surface of the prepreg sheet and the laminate is heated. Circuit patterns are then formed. Multilayered laminates are made using aramid-epoxy

sheets (prepreg) which consists of thermosetting epoxy and glass cloth. Copper foil is then placed onto the substrates and circuits are constructed. Takanaka et al also teaches that organic material can also be used to make the prepreg sheets. Ehman et al teach *inter alia* mounting electronic components on a resin layer. It would have been obvious to one of ordinary skill in this art to combine the two teachings and to provide electronic components on the substrate taught by Takanaka et al rather than circuits and thereafter completely cure the semi-cured resin sheet with the electronic components buried therein.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to C. J. Arbes whose telephone number is 571-272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P. Vo, can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CARL J. ARBES
PRIMARY EXAMINER